Ewen Crawford

Queen's University

Bachelor of Applied Science, Computer Engineering

• Coursework: Digital Design, Computer Networks, Data Structures, Signals and Systems.

WORK EXPERIENCE

Marvell – Design Verification Intern

- Worked alongside Marvell's Ethernet IP division to further support implementation of the IEEE 802.1AE (MACsec) standard by applying formal verification methods.
- Responsible for verifying a low-latency statistics engine used to provide general channelized accounting across large counter domains.
- Built a synthesizable reference model, against which behavioural properties were specified with SVAs and design correctness exhaustively proven with Cadence's Jasper FPV proof-solver app.
- Delivered a presentation to the executive leadership team as a part of a small intern group.

Trend Micro – Vulnerability Research Intern

- Investigated remote code execution vulnerabilities in production software by using WinDbg to help locate exploitable code in binaries disassembled and decompiled with Ghidra.
- Authored reports for 0-day and N-day security flaws, which included creating functional proofof-concepts to demonstrate an attack on the reported vulnerabilities.
- Produced regex-based filters to detect malicious network traffic at customer endpoints.

PROJECTS

Ethernet MAC

- Currently working on a SystemVerilog implementation of an IEEE 802.3 compliant MAC.
- Designed and verified an asynchronous FIFO to cross data between L3 and L2 clock domains.
- Code available at *https://github.com/eacrawford02/eth-mac*

FPGA Lava Lamp

- Designed a digital replica of a lava lamp on a Xilinx Artix-7 FPGA using SystemVerilog.
- Implemented the metaball algorithm in hardware with fixed-point arithmetic to describe simulation behaviour.
- Wrote a display controller to drive an LED matrix panel with the simulation output.
- Code and demonstration available at https://github.com/eacrawford02/lava-lamp

SKILLS & INTERESTS

Technologies: Vivado, Cadence Jasper RTL Apps, Git, SQL, HTML & CSS, Linux

Languages: Verilog/SystemVerilog, C/C++, Python, Java, Dart, Tcl

Interests: Formal verification, FPGAs, graphics programming, applied probability

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Expected Graduation: April 2024

May 2023 - Aug. 2023

May 2022 - Aug. 2022

Aug. 2022 – Mar. 2023

July 2023 - Present